IMEC 65 nm test structures
Total Ionizing Dose Irradiation Test Report, V2.0

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1 Introduction

This document presents the total ionizing dose (TID) irradiation tests results performed on 65 nm test structures from IMEC**.** This work was performed in the frame of NEPP project.

2 Test structures

NMOSFETs and PMOSFETs have been fabricated in IMEC 65 nm CMOS technology using a 1.4 nm gate oxide. Devices with a fixed width W=10 µm have been mounted in 24-pin dual in line packages. Transistors with separate gate and drain contacts that belong to a short length array were selected. Five gate lengths ranging from 0.13 µm to 0.25 µm are available. All five NMOS transistors share a common source. All five PMOS transistors share a common source. Figure 1 shows test device pinout.

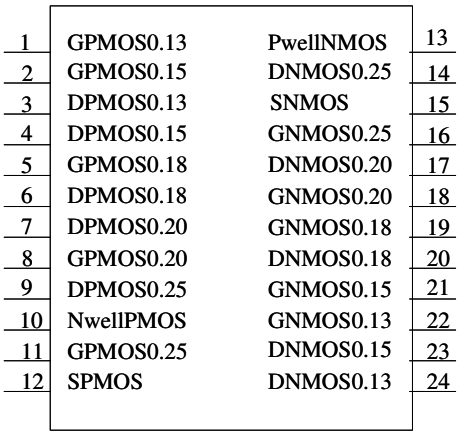

Figure 1: test device pinout

IMEC provided 10 test devices samples as described above; however, because of poor bonding yield, only a few transistors per device are functional. Tables 1 identifies the functional transistors, the functional but leaky transistors, and the non-functional transistors for each test sample. Table 1 shows the status as it was observed at NASA GSFC during initial pre-irradiation measurements. It should be noted that we found less functional transistors than IMEC. This indicates the high sensitivity to handling of test samples. Other failures were observed during the tests that we can not attribute to radiation effects (see paragraph 7).We can see that we have a very small number of fully functional transistors. For P channel transistors we only have one 0.13µm gate length transistor, two 0.15µm gate length transistors, zero 0.18 µm gate length transistor, zero

0.2 µm gate length transistor, and four 0.25 µm gate length transistors. For N channel transistors the situation is a little bit better with one 0.13µm gate length transistors, two 0.15µm gate length transistors, four 0.18 µm gate length transistors, four 0.2 µm gate length transistors, and zero 0.25 µm gate length transistor.

Table 1: identification of functional, leaky, and non-functional transistors

Type	Gate Length	Part number									
		LEW8-1	LEW8-2	LEW8-3	LEW8-4	LEW8-5	LEW8-6	LEW8-7	LEW8-8	LEW8-9	LEW8-10
PMOS	0.13	functional	not functional	not functional	not functional	leaky	leaky	not functional	leaky	leaky	not functional
	0.15	not functional	not functional	not functional	not functional	functional	not functional	functional	not functional	not functional	leaky
	0.18	not functional	not functional	not functional	leaky	leaky	leaky	not functional	not functional	not functional	not functional
	0.2	not functional	not functional	not functional	not functional	not functional	not functional	not functional	not functional	not functional	not functional
	0.25	functional	not functional	not functional	not functional	functional	leaky	functional	not functional	functional	leaky
NMOS	0.13	not functional	not functional	not functional	leaky	leaky	not functional	leaky	not functional	functional	not functional
	0.15	functional	leaky	leaky	leaky	leaky	leaky	functional	not functional	subth leak	leaky
	0.18	functional	functional	leaky	leaky	leaky	leaky	functional	not functional	subth leak	functional
	0.2	leaky	functional	leaky	leaky	functional	leaky	functional	not functional	functional	leaky
	0.25	not functional	not functional	not functional	not functional	leaky	not functional	Id leak	not functional	not functional	leaky

3 Irradiation Conditions

8 devices were be exposed using the GSFC Co^{60} source per MIL-STD-883 Method 1019.6; two devices were used as control parts. Dose levels were 20, 40, 80, 150, 300, 500, and 1000 krad (Si). Four devices were irradiated at a high dose rate greater than 1 rad (Si)/s. Four devices were irradiated at a low dose rate of 0.1 rad (Si)/s. Actual irradiation test sequences are shown in Appendixes. After the end of irradiation all parts were submitted to one week room temperature annealing.

4 Bias conditions during irradiation

During exposure, three out of the four devices were biased. One test sample was unbiased with all terminals grounded. On the biased devices, all transistors were biased on with 1.2V gate voltage, all other terminals being grounded as shown in Figure 2. Test samples irradiation and biased conditions are shown in Table 2.

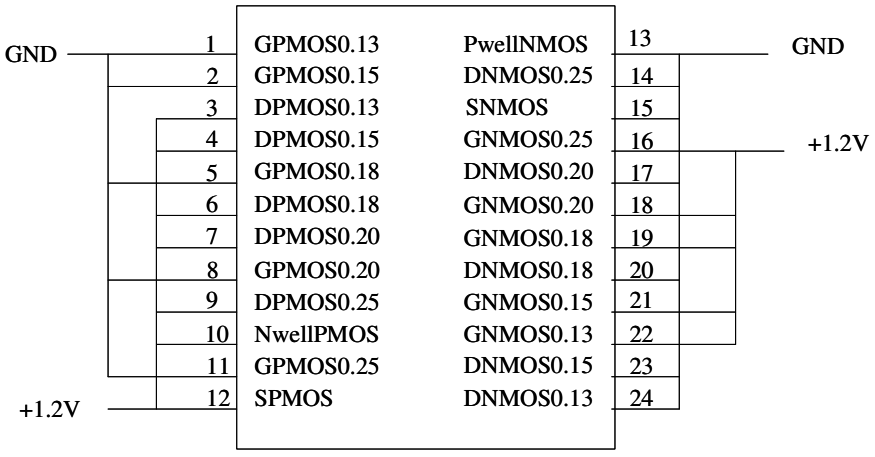

Figure 2: exposure bias circuit

Table 2: Irradiation and bias conditions of each test sample

	LEW8-1	LEW8-2	LEW8-3	LEW8-4	LEW8-5	LEW8-6	LEW8-7	LEW8-8	LEW8-9	LEW8-10
Irradiation condition	High dose rate	High dose rate	High dose rate	High dose rate	Low dose rate	Low dose rate	Low dose rate	Low dose rate	control	control
Bias during irradiation	on	on	on	unbiased	unbiased	on	on	on	control	control

5 Test conditions

Before irradiation, at each dose level, and after annealing, the standard transistor characteristics of all the devices, including the control parts, were measured with a Keithley 4200 parametric analyzer:

- Id versus Vgs, Vgs varying from –1.2V to +1.2V with Vds=0.025V and Vds=1.2V
- Ig versus Vgs, Vgs varying from –1.2V to +1.2V with Vds=0.025V and Vds=1.2V
- Id versus Vds, Vds varying from 0V to +1.2V with Vgs=0.4V, Vgs=0.6V, and Vgs=0.8V

6 Test Results

Drain source current Ids versus gate source voltage Vgs characteristics did not change significantly with radiation up to the maximum tested dose level of 1 Mrad-Si. For example, Figures 1 and 2 show the Ids versus Vgs characteristics for 0.2 µm gate length NMOS transistor. We cannot see any degradation of characteristics with dose.

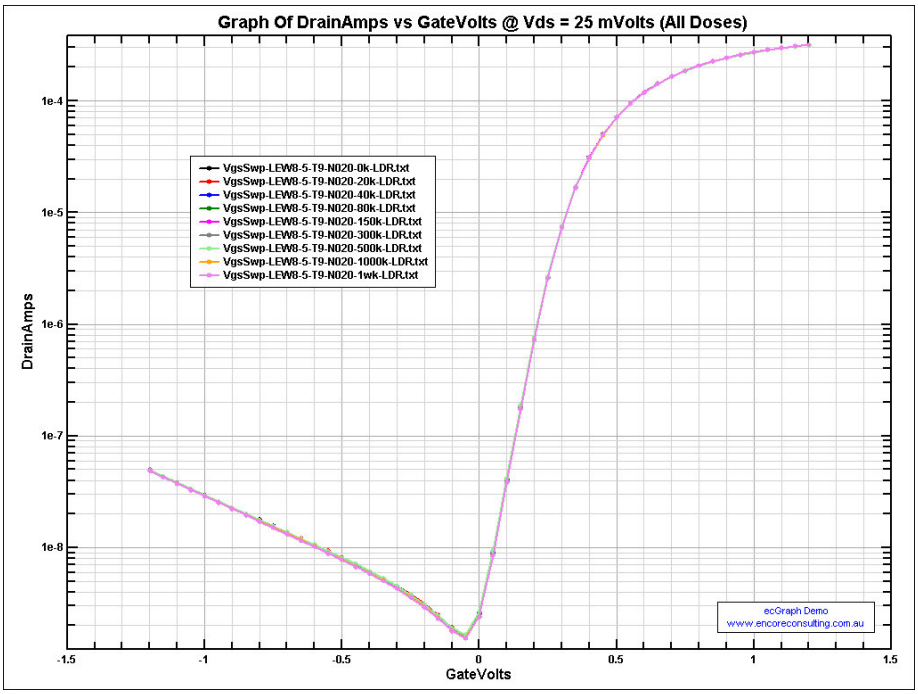

Figure 1: 0.2 µm gate length NMOS transistor,
degradation of Id=f(Vgs) @ Vds=25mV characteristics with dose

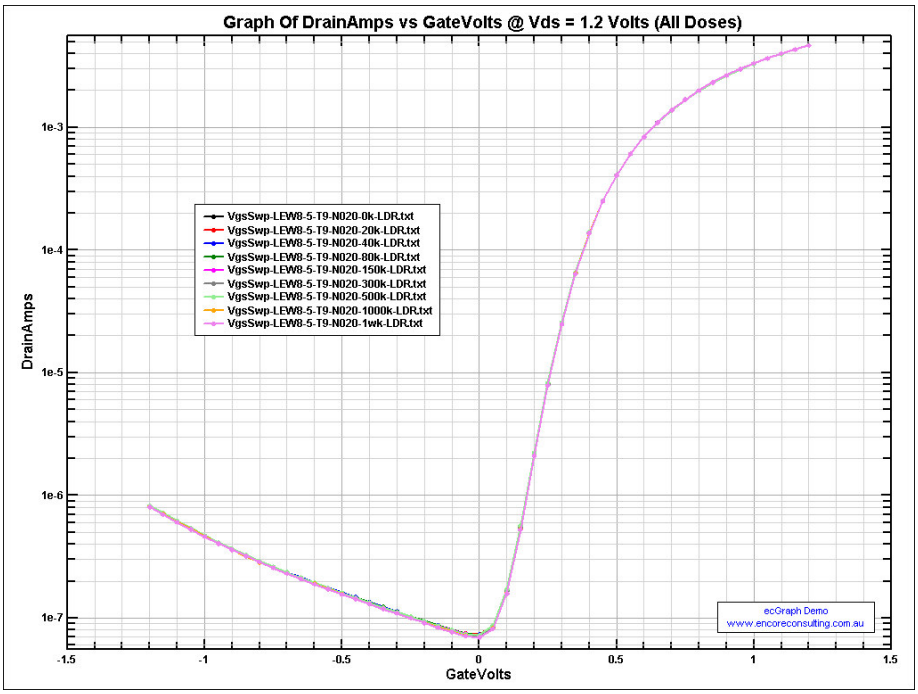

Figure 2: 0.2 µm gate length NMOS transistor,
degradation of Id=f(Vgs) @ Vds=1.2V characteristics with dose

Figures 3 and 4 show the Ids versus Vgs characteristics for 0.15 µm gate length PMOS transistor. We cannot see any degradation of characteristics with dose.

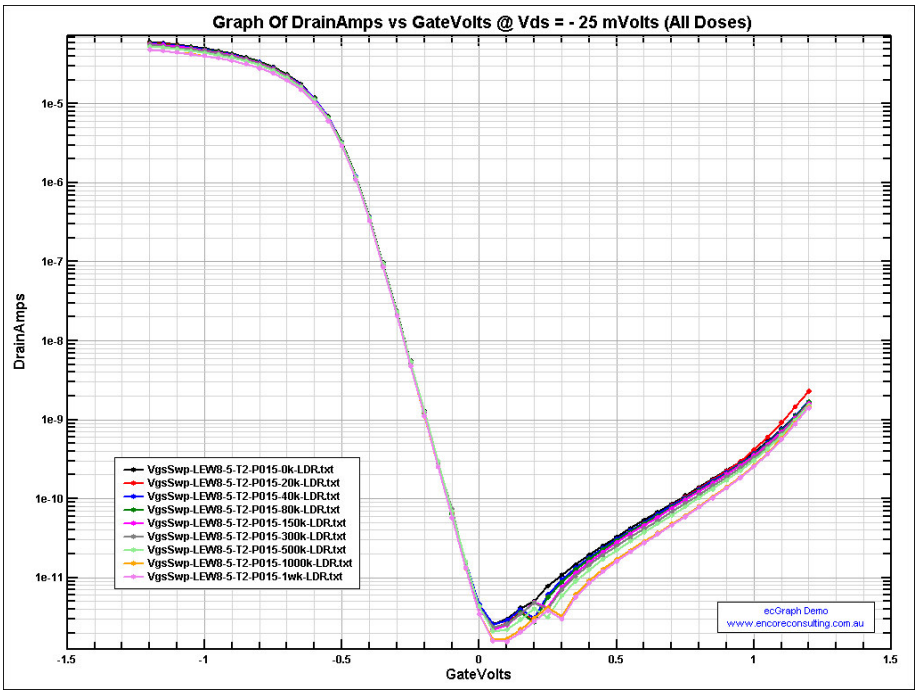

Figure 3: 0.15 µm gate length PMOS transistor,
degradation of Id=f(Vgs) @ Vds=-25mV characteristics with dose

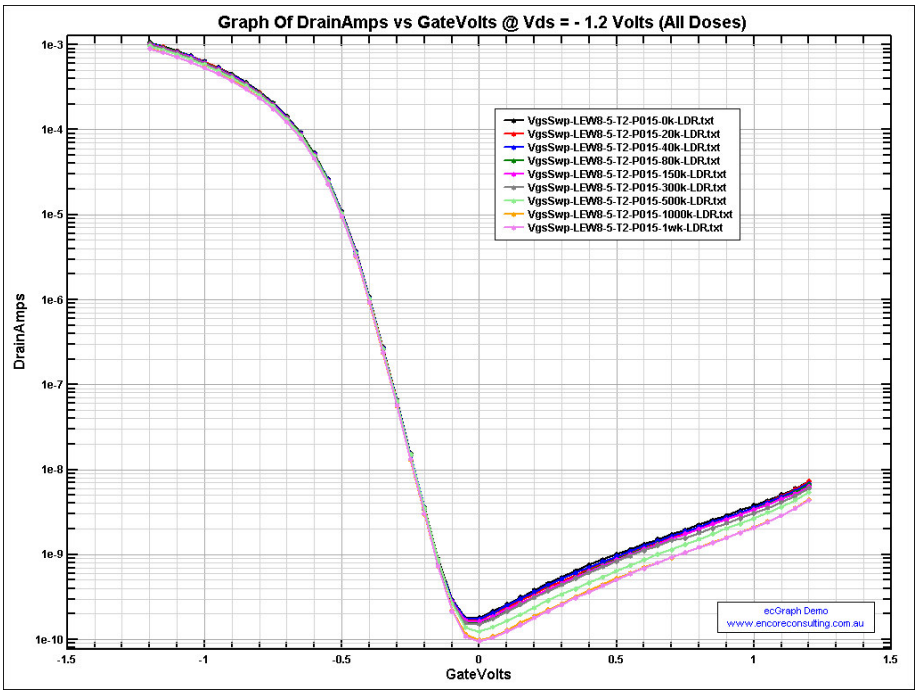

Figure 4: 0.15 µm gate length PMOS transistor,
degradation of Id=f(Vgs) @ Vds=-1.2V characteristics with dose

Figure 5 shows Igs versus Vgs characteristics for 0.2 µm gate length NMOS transistor.

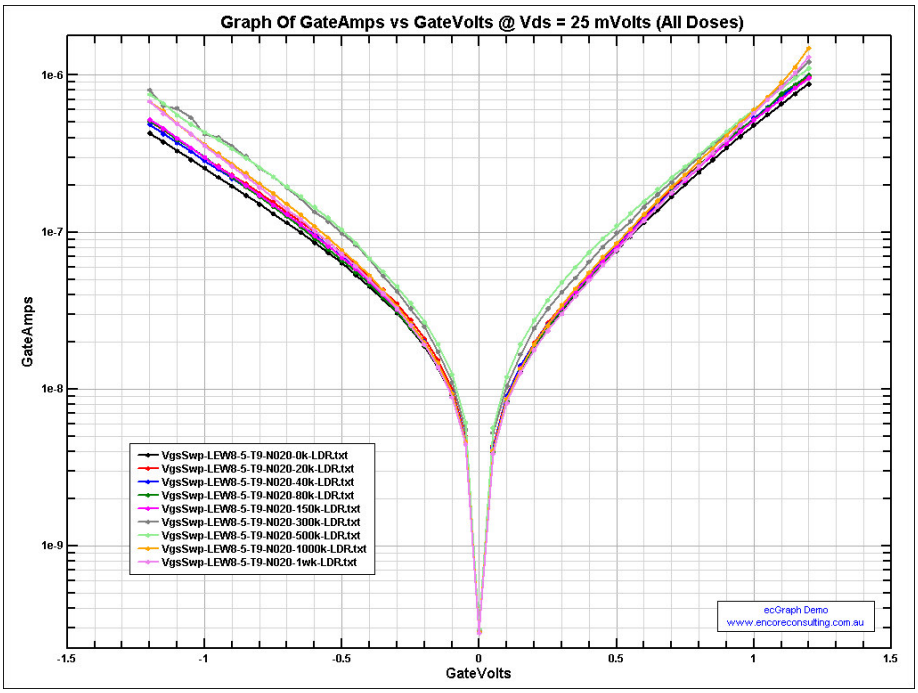

Figure 5: 0.2 µm gate length NMOS transistor,
degradation of Ig=f(Vgs) @ Vds=25 mV characteristics with dose

Figures 6 and 7 show Igs versus Vgs characteristics for 0.15 µm gate length PMOS transistor.

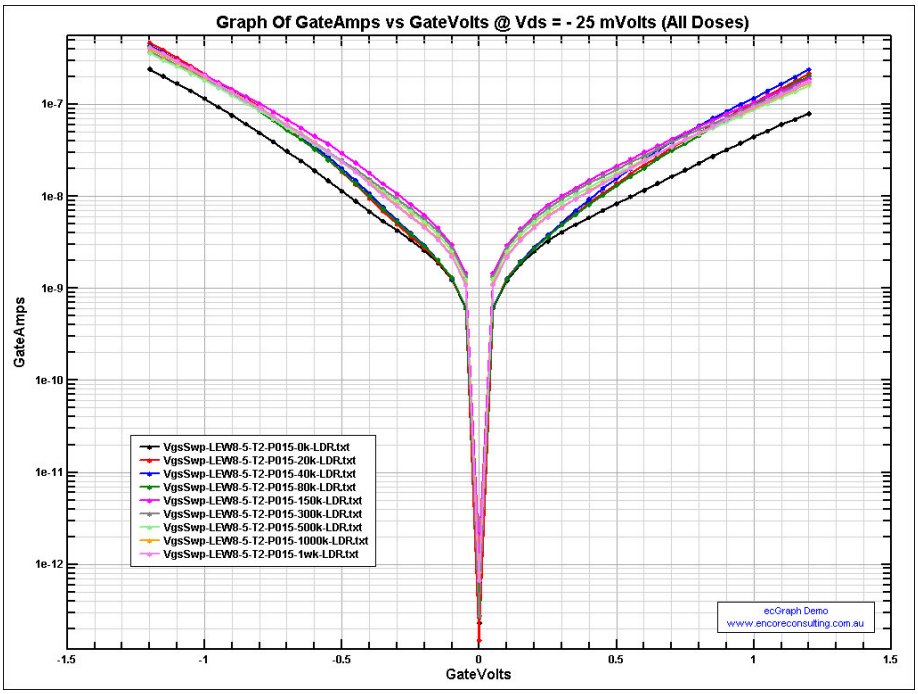

Figure 6: 0.15 µm gate length PMOS transistor,
degradation of Ig=f(Vgs) @ Vds=-25mV characteristics with dose

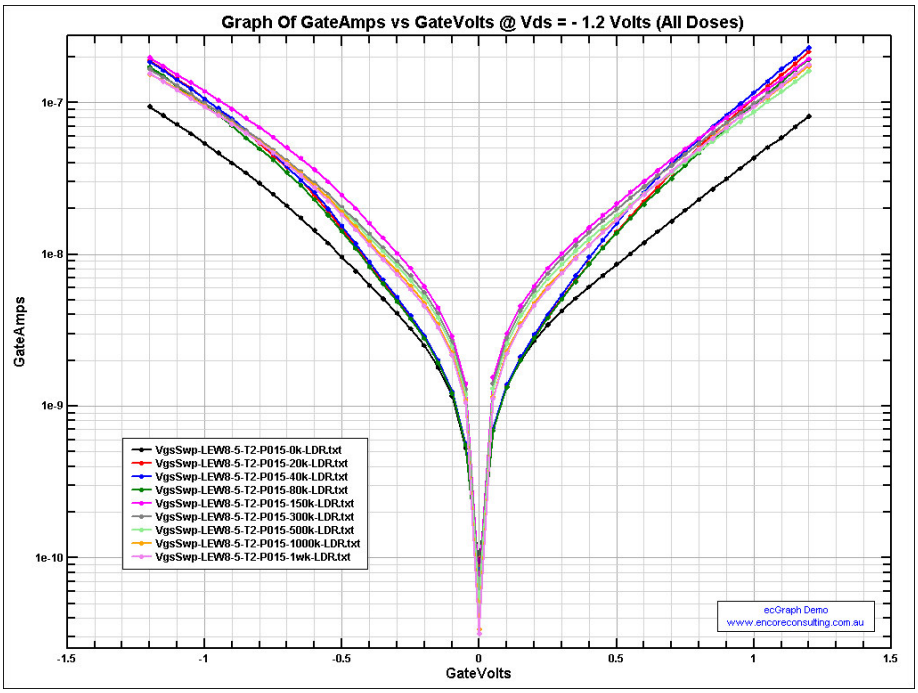

Figure 7: 0.15 µm gate length PMOS transistor,
degradation of Ig=f(Vgs) @ Vds=-1.2V characteristics with dose

We can see in Figures 5 to 7 a small increase of gate current with dose. Currents increase consistently with dose levels except for the last dose level at 1 Mrad-Si. This last measurement was performed 24 hours after the end of irradiation (see section 7). It is possible that an annealing occurred. Figure 8 shows Igs versus Vgs characteristics for 0.18 µm gate length PMOS transistor. This transistor was initially leaky. We can see a larger increase of gate current with dose especially after 500 Krad-Si.

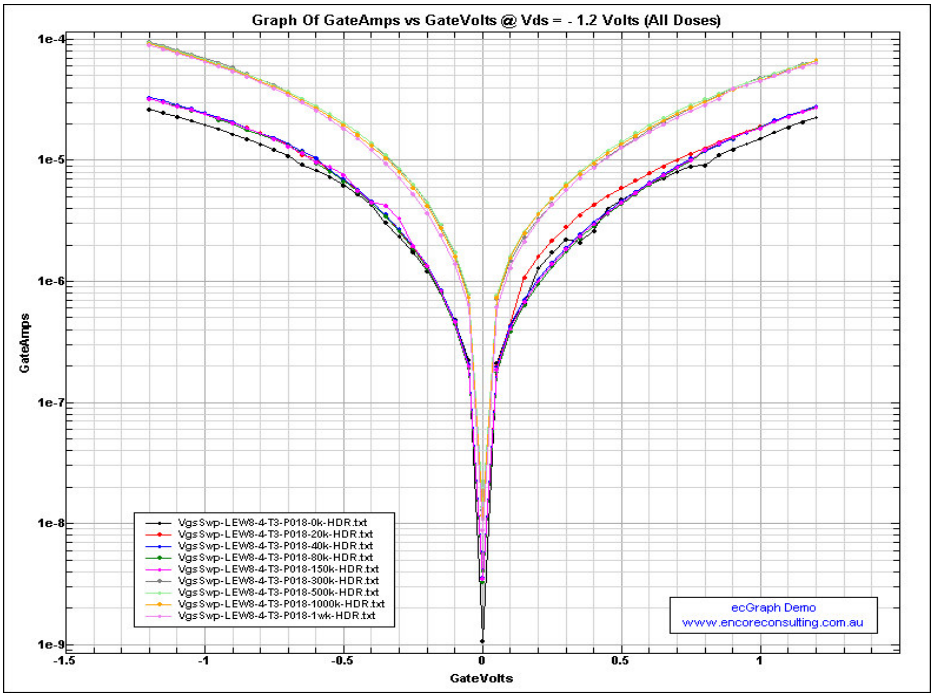

Figure 8: 0.18 µm gate length PMOS transistor,
degradation of Ig=f(Vgs) @ Vds=-1.2V characteristics with dose

Larger degradations were observed on other parts. For example, Figure 9 shows the degradation of gate current on a 0.18 µm gate length NMOS transistor. We can see a large increase, about one order of magnitude, after 300 and 500 Krad-Si. The other characteristics of this transistor do not show any degradation as can be seen in Figure 10. Several other parts show large increases of gate current starting at 150 Krad-Si. However, we don't have enough data to state with certainty that all these degradations were caused by dose effects. Some data obtained do not look consistent with TID degradation. See next section.

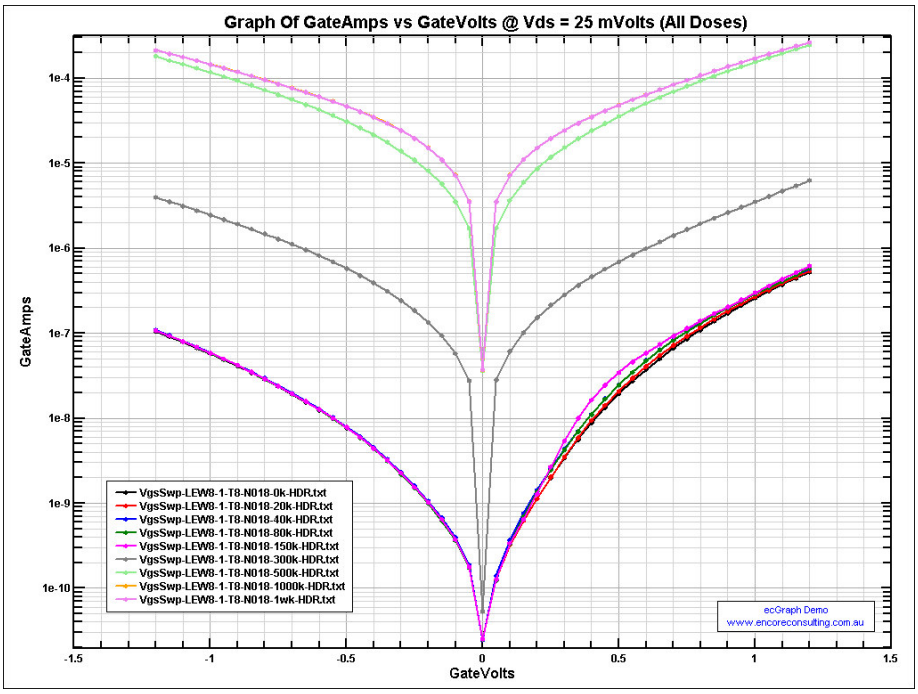

Figure 9: 0.18 µm gate length NMOS transistor,
degradation of Ig=f(Vgs) @ Vds=-25mV characteristics with dose

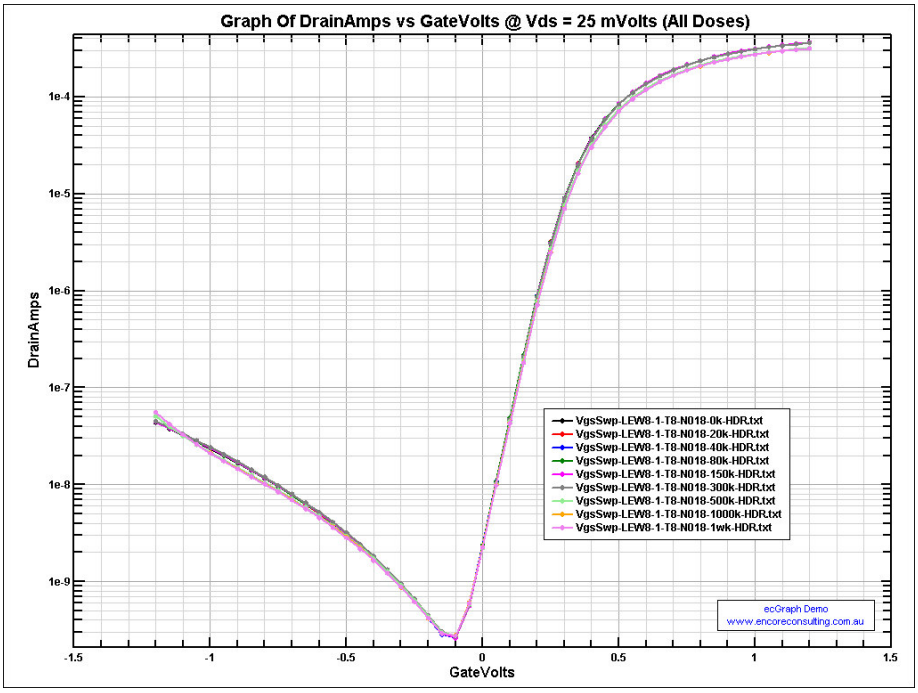

Figure 10: 0.18 µm gate length NMOS transistor,
degradation of Ids=f(Vgs) @ Vds=25mV characteristics with dose

7 Problems encountered and anomalies

- During low dose rate test, the last measurement after 1 Mrad-Si was performed 24 hours after the end of irradiation. This may explain the apparent annealing observed in Figures 6 to 8.
- Some degradations are clearly not consistent with irradiation effects. This especially true for control parts that should not show any variation of characteristics. Figure 11 shows an example of a control transistor. We can see in the Figure that all characteristics are on top of each other during the high dose rate test. But in Figure 12, we can see on the same transistor also used as a control part for the low dose rate test an increase of gate current after the last 2 measurement steps. It is possible that we have in this case an oxide breakdown induced by ESD. We don't have enough statistics to rule out the same problem on irradiated parts. All test samples provided has shown a very high sensitivity to handling and ESD even though all tests were performed on ESD protected test stations. For example, during the low dose rate test, the 150Krad-Si measurements were performed on a test station without ionizer. Four transistors died during this test and several others showed large increases of gate current.

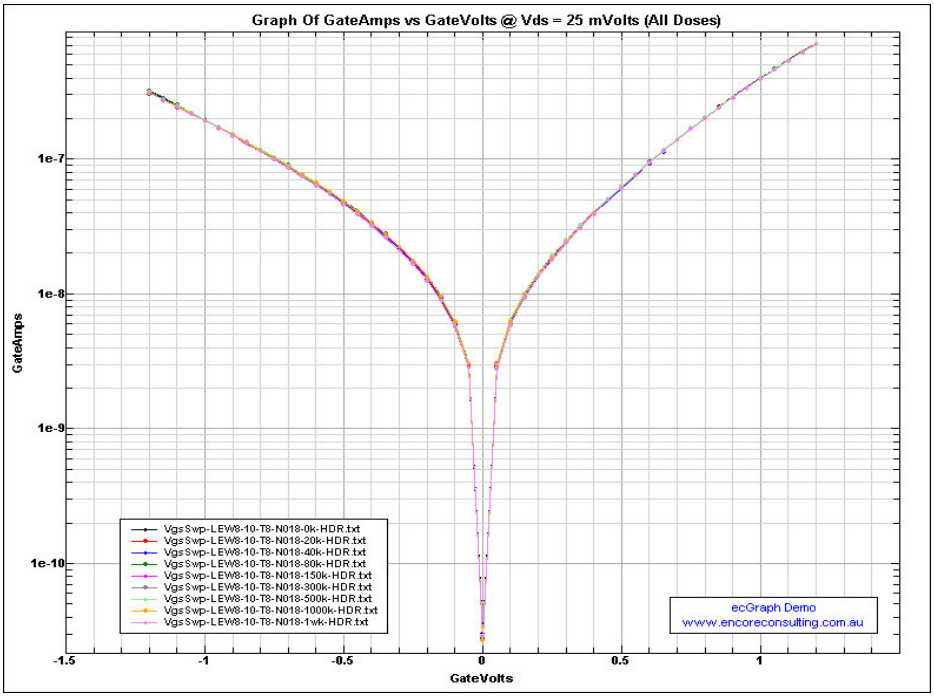

Figure 11: 0.18 µm gate length NMOS transistor, Ig=f(Vgs) @ Vds=-25mV characteristics, this transistor was a control part, dose levels indicates the irradiation steps after which the control part was measured along with irradiated parts

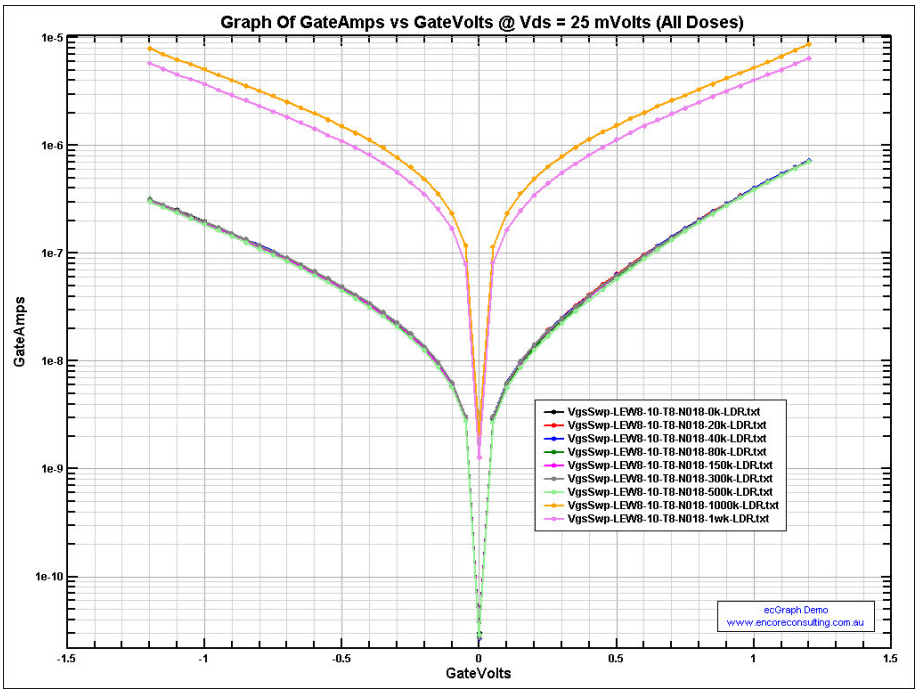

Figure 12: 0.18 µm gate length NMOS transistor, Ig=f(Vgs) @ Vds=-25mV characteristics, this transistor was a control part, dose levels indicates the irradiation steps after which the control part was measured along with irradiated parts.

8 Conclusions

No degradation of drain current versus gate voltage characteristics were observed on all irradiated parts up to a total dose of 1 Mrad-Si.

Increases of gate currents were observed during irradiation. We don't have enough statistics to rule out gate oxide breakdown induced by ESD. This is probably the case when large variations of gate current were observed. However, the annealing observed on some parts that show small increases of gate current (see figures 5 to7) seems to indicate that TID causes an increase of gate current.

9 Appendix 1: irradiation test sequence, high dose rate

Run #	Date/Time In	Date/Time Out	# Hours InCo60 Chamber	# Days In Co60 Chamber	Dose Received (kRad)	Accumulated Dose (kRad)	Average Dose Rate (Rad/sec)
1	10/12/06 9:33 AM	10/12/06 11:00 AM	1.45	0.060	20	20	3.83
2	10/12/06 11:56 AM	10/12/06 1:07 PM	1.18	0.049	20	40	4.69
3	10/12/06 2:07 PM	10/12/06 4:08 PM	2.02	0.084	40	80	5.51
4	10/12/06 4:45 PM	10/13/06 7:35 AM	14.83	0.618	70	150	1.31
5	10/13/06 8:10 AM	10/13/06 2:00 PM	5.83	0.243	132	282	6.29
6	10/13/06 5:40 PM	10/16/06 7:40 AM	62.00	2.583	300	582	1.34
7	10/16/06 11:08 AM	10/17/06 8:00 AM	20.87	0.869	420	1002	5.59
Totals			**108.18**	**4.51**			

10 Appendix 2: irradiation test sequence, low dose rate

Run #	Date/Time In	Date/Time Out	# Hours In Co60 Chamber	# Days In Co60 Chamber	Dose Received (kRad)	Accumulated Dose (kRad)	Average Dose Rate (Rad/sec)	Comments
1	10/13/06 5:40 PM	10/16/06 8:30 AM	62.83	2.618	20	20	0.09	
2	10/16/06 11:08 AM	10/18/06 12:08 PM	49.00	2.042	20	40	0.11	
3	10/18/06 1:32 PM	10/24/06 1:20 PM	143.80	5.992	40	80	0.08	
4	10/24/06 3:12 PM	10/31/06 10:30 AM	163.30	6.804	70	150	0.12	
5	10/31/06 1:05 PM	11/15/06 12:00 PM	358.92	14.955	150	300	0.12	
6	11/15/06 3:46 PM	12/13/06 9:00 AM	557.23	23.218	200	500	0.10	No radiation for 4.5 days due to chamber door shutoff from 11/22/06 10pm thru 11/27/06 11am (This has been taken into account)
7	12/13/06 12:10 PM	2/5/07 12:10 PM	1296.00	54.000	500	1000	0.11	measurements delayed 24 hours after end of irradiation
Totals			**2631.08**	**109.63**				